Automated Susceptibility Analysis of Single Event Transients for Combinational Cells

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***Abstract*—Effects caused by radiation have become more significant due to the trend towards circuit miniaturization, directly affecting circuits reliability. When the reliability is compromised, it can result in an unexpected behavior, such as malfunctions or signal disruptions. For this reason, an accurate evaluation of circuit reliability is essential for fault-tolerant approaches. This could enable a robust reliability-aware automated design flow. Under these conditions, this work proposes a tool capable of analyzing the radiation susceptibility for a given combinational logic gate layout design. A 45nm standard cell library is used to validate the proposed tool. As far as we know, this is the first work to propose an open-source tool for assessing susceptibility at the layout level of a cell library without electrical simulations.**

I. Introduction

Driven by the scaling down of transistors in size, circuits become more sensitive to various faults, impacting reliability directly and negatively [1]. Single event effect (SEE) characterizes the radiation-induced impact on electronic devices [2]. The SEEs under analysis in this work will encompass those that, while not causing physical damage, can disrupt information within combinational logic gates. In this regard, single event transient (SET) have the potential to alter the output signal of a combinational cell without damage [3]. Thus, it will be investigated, considering transient current pulses influenced by the particle flux and sensitive node areas. Besides that, considering the dependencies inherent to SETs, as described by [4], a layout-derived information provide deeper insights. Additionally, by analyzing logic gate layouts, a more comprehensive analysis of susceptibility to faults in the functions can be conducted [3].

Therefore, the aim of this study is to evaluate the susceptibility of combinational logic gates from a standard cell library to SETs. To achieve this objective, the main contribution of this work is provide a tool capable of extracting and computing the susceptible area of a cell at the layout level, identifying the active diffusion regions where particles may have an impact for a given input vector.

Studies utilizing a susceptibility analysis at a logic gate layout-level employed a comparable approach, but they were done manually [3] [5] [6]. Others similar studies in literature lack on providing a detailed susceptibility analysis at a cell layout-level, evaluating layout-oriented simulations of circuit blocks [7] or conducting SET analyses not at the layout level, but rather in the schematic model using SPICE simulation [4] [8] [9]. The tool introduced by [10] offers robust insights into how a cell is affected by particles at the layout level. Although the author does not specify the time required for calculations, simulating complex 3D behaviors demands significant computational power. On the other hand, the tool proposed in this study is simpler, resulting in faster calculations and easier operation. Additionally, it provides a probabilistic analysis of susceptibility in combinational logic gates, allowing for the estimation of their reliability at the layout level.

II. Background

The development of the proposed tool is based on the influence of SET on combinational logic gates. In brief, susceptibility values can be extracted from a layout file by calculating sensitive node areas, which represent the circuit's diffusion area vulnerable to particle impacts. To enable the tool to assess the reliability of a logic gate, it requires a technique capable of calculating the probability of both correct and incorrect output occurrences, considering the layout level. In this circumstances, the probabilistic transfer matrix (PTM) proposed by [11] could be a good option as it does not require significant computational power, which is noteworthy taking into account that circuit testing is a high-cost task [5]. However, this method does not consider individual logic gate designs [3] and assumes a uniform error probability values for all of them [5]. Hence, the layout method proposed by [3] emerges as the most promising technique, as it harnesses the advantages of PTM while incorporating cell-specific design considerations. For this purpose, the author also proposed a gate's susceptibility equation, which is utilized in this study. These concepts are summarized in the next subsections.

A. Influence of SETs in combinational logic gates

Less abundant charge carriers are generated when a charged particle strikes a silicon bulk. These minority carriers are collected by the source/drain diffusion nodes and, consequently, alters their logic state [12]. This phenomenon, known as SET, influences the circuit during a time interval [9].

In CMOS circuits, this disruption turns on the parasitic bipolar transistors between well and substrate [13]. In other words, a sensitive node, in this transistor technology, is the reverse-biased PN junction [7] [3].

B. Probabilistic transfer matrix

In a world without malfunctions and errors, a Truth Table could represent perfectly the behavior of a combinational cell

[5]. However, a incorrect output may occur due to single event effects. In this context, the PTM can be used to map each input vector to a correspondent probability of success and failure, associated with a logic gate behavior [11]. In other words, there are two columns for each input vector, denoting the probability of yielding a logical zero and one. For example, for an AND gate, the input "01" results in a logical zero. In its PTM, this input correspond to $1 - p$ and p, column zero and one, respectively. The variable p denotes the gate's susceptibility.

In this work, a PTM can be generated in a flattened or unflattened file, both in TXT format. In the unflattened file, the first row indicate the logic gate, each row subsequently represents an input vector and the columns indicate the probability of obtaining a logical zero and one. In the flattened file, all the content is displayed on a single line. It starts with the cell name, followed by the values of each row in sequential order, left to right and then from top to bottom.

C. Susceptibility equation

In this study, the susceptibility of a logic gate is defined by Eq. 1 [3], where Δ is the summation of the sensitive node areas, representing the portion of the circuit's active diffusion area that is susceptible to the occurrence of a particle for a given input vector; and ϕ is defined as the particle incidence rate per nm^2 in one hour of operation. The computation of Δ stands as the essential objective of this work. About ϕ value, the particle flux is ≈ 100 particle per $cm^2 * sec$ at high-altitude and ≈ 1 particle per $cm^2 * sec$ at sea level [2]. Readjusting these values for hours and nanometers, it is obtained $\phi = 3.6 * 10^{-9}$ and $\phi = 3.6 * 10^{-11}$, respectively. The ϕ value used in this work is 3.6E-09, the particle flux of aircraft level.

$$p = \Delta * \phi \tag{1}$$

III. Methodology

To assess the susceptibility of logic gates, this work developed a flow described in Figure 1. About the tool flow, it can be segmented into four main steps. Beginning with the "Input Data" segment, the user informs what combination logic gate layout file is going to be analyzed. The layout format file is the graphic data system II (GDSII), used by foundries for IC fabrication [10]. The GDS files describe a circuit at the layout level using polygons to represent various components such as active diffusion, connectors, metals, polys, and others. In this work, the tool uses GDS files from the 45nm FreePDK provided by NANGATE. Additionally, as one of the tool's input and due to the multiple particle flux calculation options, users have the flexibility to specify their preferred value.

The program was built with CMOS technology in mind. For this reason, Step 2 prepares the simulation environment by constructing two graphs: one for the NMOS part and another for the PMOS part, both of which contribute to building the circuit graph. To achieve this, the GDS file supplies all the cell polygons. Only those belonging to layers of interest, as active diffusion, connector, metal and poly, are extracted

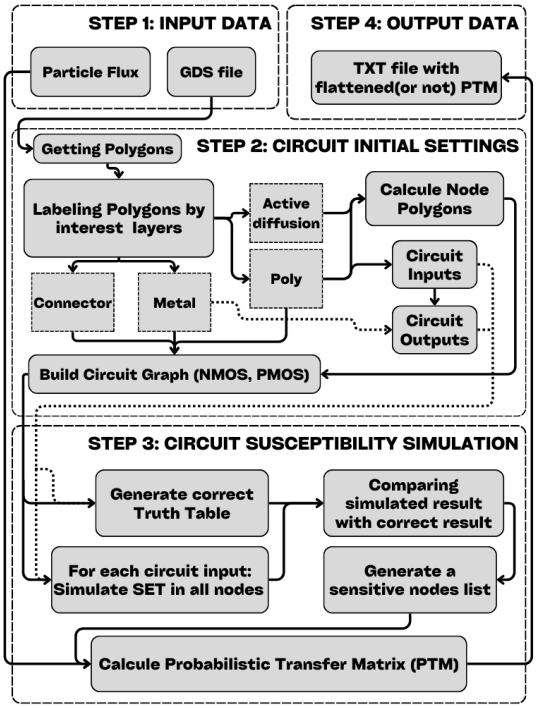


Fig. 1. Susceptibility tool flow diagram

and categorized. Node polygons can be determined through mathematical comparisons between active diffusion and poly polygons. It is important to emphasize that the nodes are the active diffusion's area susceptible to particles impact. Lastly, circuit inputs and circuit outputs are obtained, by inspecting the poly polygons data and by comparing the calculated inputs with the metal polygons data, respectively.

In Step 3, the tool simulates the cell's behavior using a breadth-first search (BFS) algorithm within the circuit graph. With this, a Truth Table can be generated to represent the expected output for each input vector. Subsequently, for each input, a SET is simulated in each node and it is verified whether the output changes. If so, nodes that influence the output are identified as sensitive. As a result, a list of sensitive node polygons for each input is generated and, consequently, the PTM is calculated. The tool's SET simulation simply presupposes that a particle with sufficient energy affects a node, assuming that the transistor leading to this node is ON/Closed. However, nodes connected to VDD or VSS are not sensitive, as these power supply voltages provide an energy level that is considered too high for particle interference.

Lastly, on Step 4, the tool provides the user with a TXT file containing the calculated PTM. The generated PTM can be used to calculate reliability in larger circuits, with many logic gates interconnected. In this cases, this output could be easily used as a input for another tool to perform a more complex reliability calculation.

This flow adopts the Python programming language for its ease of use and readability. Additionally, a library named GDSTK was utilized to enable the software to read a GDS

file, while the KLayout tool was used for better visualization of layouts.

IV. Results

To showcase the potential use of the proposed tool, this work presents some experiments considering thirty combinational logic gates from the 45nm FreePDK presented in Table I. In order to validate the tool developed in this work, the results presented here will focus on two analyses: A) runtime and B) the evaluation of each cell against the impact of SET failures. Each cell was evaluated for each possible input vector. Only HA and FA cells feature two outputs, thus, in this case, both susceptibility values are considered.

A. Runtime evaluation

For one hour and six minutes, ten thousand simulations were conducted for each cell, recording the execution time they need to traverse all segments of the tool's flow. The machine utilized features a 13th Gen Intel(R) Core(TM) i5-13450HX 2.40 GHz processor and 16 GB of RAM memory. Among the cells analyzed, as shown in Figure 2, it is noted that the area of the logic gate has a greater impact than the number of inputs. For example, compared to 6-input cells such as AOI222, OAI222, and OAI33, the FA cell took nearly 0.02 seconds longer to generate a result, despite having half the number of inputs. Alternatively, when comparing cells with the same number of inputs, such as NAND2 and AND2, those with a larger area tend to take more time.

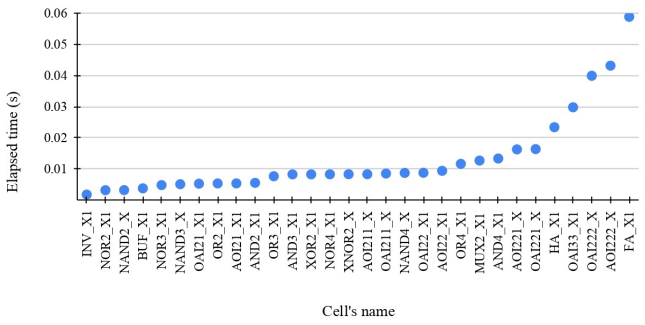


Fig. 2. Tool's runtime, from reading a GDS file to generating the PTM

The cause may lie in the simulation process, during Step 3. Conducting a BFS in the circuit graph inevitably results in a path reaching the final metal, either through the NMOS or the PMOS. Having a larger area, a cell consequently has more polys, metals, connectors, and/or nodes to cross, leading to a longer runtime.

B. 45nm standard library cell evaluation

The developed tool can extract and compute the susceptible area of cell's active diffusion, where particles may impact given an input vector. With this at hand, basic statistics were conducted to calculate the minimum, average, and maximum susceptibility values, as well as the standard deviation, presented in Table I.

TABLE I
CELLS UTILIZED (SUFFIX X1 OMITTED), THEIR RESPECTIVE INPUTS, AREA(μm^2), SUSCEPTIBILITY METRICS (IN 10^{-5}) AND STANDARD DEVIATION (σ) COMPUTED USING THE DEVELOPED TOOL

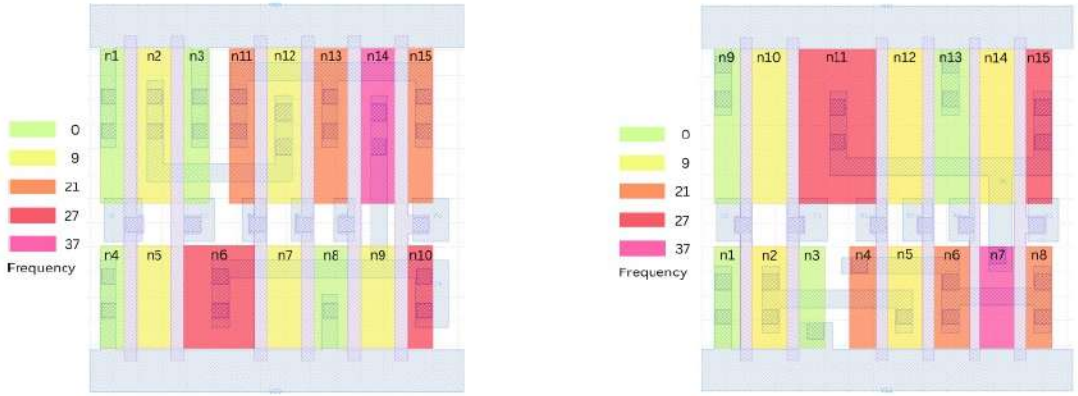
Cell	INP.	Area	Minimum	Mean	Maximum	σ
INV	1	0.6	15.69	19.75	23.81	4.06
BUF	1	0.89	27.59	29.67	31.75	2.08
NAND2	2	0.89	15.69	24.93	36.6	9.45
NOR2	2	0.89	20.92	31.03	55.57	14.22
AND2	2	1.19	31.56	34.35	42.34	4.61
OR2	2	1.19	27.59	33.26	43.47	6.51
XNOR2	2	1.79	20.92	54.01	73.4	21.15
XOR2	2	1.79	31.75	58.02	97.9	24.42
HA	2	2.98	63.32	92.37	129.65	24.44
AOI21	3	1.19	20.92	51.14	87.32	28.71
NAND3	3	1.19	15.69	31.13	57.52	16.98
NOR3	3	1.19	23.81	41.29	87.32	21.71
OAI21	3	1.19	20.92	42.67	63.5	16.88
AND3	3	1.49	31.75	38.51	52.92	7.45
OR3	3	1.49	27.59	37.37	59.35	10.98
MUX2	3	2.09	31.56	44.56	56.89	11.63
FA	3	4.77	64.26	86.03	109.43	14.88
AOI211	4	1.49	31.75	71.18	119.07	32.82
AOI22	4	1.49	20.92	48.38	111.13	31.93
NAND4	4	1.49	15.69	33.06	78.44	20.38
NOR4	4	1.49	23.81	46.77	119.07	28.58
OAI211	4	1.49	20.92	53.91	87.32	21.45
OAI22	4	1.49	20.92	48.72	95.26	23.83
AND4	4	1.79	31.75	40.01	63.5	9.71
OR4	4	1.79	27.59	39.6	75.22	14.34
AOI221	5	1.79	31.75	68.29	142.88	33.68
OAI221	5	1.79	20.92	57.2	119.07	26.27
OAI33	6	2.09	31.75	67.54	158.76	32.4
AOI222	6	2.39	31.75	87.05	174.64	45.79
OAI222	6	2.39	20.92	88.71	190.51	46.84

It is worth noting that HA and FA cells exhibit a mean value approximately two to four times greater than other cells with the same number of inputs. This disparity arises from their complexity. In this circumstance, it can be observed that there is a correlation among three factors in determining a cell's total susceptibility: the number, size, and frequency of sensitive nodes across all input vectors.

In CMOS technology, PMOS transistors normally are wider than NMOS transistors, impacting directly on their node areas. As a consequence, due to the Δ, in Eq 1, be highly proportional with the size of the sensitive areas, sensitive nodes in the pull-up plane have often a greater impact on susceptibility. Using the INV_X1 cell as an example, this libray has a PMOS width equal to 0.63 μm and a NMOS width equal to 0.415 μm.

For a more detailed analysis, AOI222 and OAI222 were chosen due to their highest standard deviation susceptibility values. As a matter of visualization, Figure 5 items a) and b) are heat maps illustrating the frequency at which each node can affect the logic gate output, the higher the value, the greater the criticality. It is expected to observe that nodes connected to the output are the ones with the highest repeatability. In AOI222, nodes that have the most impact are n6, n10 and n14. In OAI222, the most frequent nodes are n7, n11 and n15.

Another important aspect is to relate what happens in their worst and best cases. This allows us to understand how these scenarios impact their susceptibility. For both cells, the input vector order is A1A2B1B2C1C2. In AOI222, the worst case



(a) AOI222_X1 (b) OAI222_X1

Fig. 3. Heat maps representing frequency of sensitive nodes across all input vectors in logic gates

always occurs when output "0" is expected and there is a connection between the output node (n14) and node n12. In these situations, the node n2 and nodes n11 to n15 are sensitive, resulting in $p = 174.636 * 10^{-5} particle/h$. On the other hand, the best case occurs when inputs A1A2 = 11, in which case only node n14 is sensitive, resulting in $p = 31.752 * 10^{-5} particle/h$. In OAI222, the worst case occurs in the input vector = 010101, resulting in $p = 190.512 * 10^{-5} particle/h$. In this situation, nodes ranging from n10 to n12 and n14 to n15 are sensitive. On the other hand, the best case occurs when inputs A1A2 = 00, in which case only node n7 is sensitive, resulting in $p = 20.916 * 10^{-5} particle/h$.

V. Conclusion

The objective of this work was to analyze the susceptibility of combinational logic gates to single event transients. As a result, a tool was developed to calculate the portion of the circuit's active diffusion area that is susceptible. In addition, the occurrence of particle impacts was tested and validated using thirty GDS files from the 45nm FreePDK provided by NANGATE. With this at hand, this tool can provides a cell reliability estimation and assist in decision-making regarding the use of layout-level fault tolerance techniques under SET.

At this moment, the tool is specifically tailored to work with the 45nm FreePDK, as other technologies necessitate distinct methods for handling cell polygons. Hence, a prospective objective is to enhance Step 2 of the tool's flow, with the aim of achieving technology-agnostic sizing. In this regard, it would be ideal for the tool to also support various transistor technologies, such as FINFET and others.

The next steps include analyzing complex circuits considering the susceptibility values of the logic gates used and their connections, and finding a correlation between the particles energy required to impact the sensitive node areas. Thereby, it would be possible to infer the degree to which expanding the area of a logic gate is worth, considering the necessary current energy and frequency of particle flux.

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